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Description generated with very high confidence

**Course Plan**

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| **Department :** | Computer Science and Engineering |
| **Course Name & code :** | **DIGITAL SYSTEM DESIGN** & **CSE 2153** |
| **Semester & branch :** | III & CSE |
| **Name of the faculty :** | Dr. Hemalatha S |
| **No of contact hours/week:** | |  |  |  |  | | --- | --- | --- | --- | | **L** | **T** | **P** | **C** | | 3 | 1 | 0 | 4 | |

**Course Outcomes (COs)**

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|  | ***At the end of this course, the student should be able to:*** | **No. of Contact Hours** | **Marks** |
| CO1: | Describe the operations of basic logic gates and implementation technology, apply k-map to simplify logical expressions, implement and analyse the performance of logic functions in various forms. | 7 | 15 |
| CO2: | Design and analyse arithmetic circuits and combinational circuits using multiplexers, encoders, and decoders. | 14 | 29 |
| CO3: | Discuss about the types of flip-flops and use them to design synchronous and asynchronous sequential circuits for different applications. | 17 | 36 |
| CO4: | Design systems like simple processor, bit counting circuit | 10 | 20 |
| CO5: | Click or tap here to enter text. | Hrs. | Marks |
|  | **Total** | 48 | 100 |

**Assessment Plan**

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| **Components** | **Assignments** | **Sessional Tests** | **End Semester/**  **Make-up Examination** |
| **Duration** | 20 to 30 minutes | 60 minutes | 180 minutes |
| **Weightage** | 20 % (4 X 5 marks) | 30 % (2 X 15 Marks) | 50 % (1 X 50 Marks) |
| **Typology of Questions** | Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation | Knowledge/ Recall; Understanding/ Comprehension; Application | Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation |
| **Pattern** | Answer one randomly selected question from the problem sheet (Students can refer their class notes) | MCQ: 10 questions (0.5 marks)  Short Answers: 5 questions (2 marks) | Answer all 5 full questions of 10 marks each. Each question may have 2 to 3 parts of 3/4/5/6/7 marks |
| **Schedule** | 4, 7, 10, and 13th week of academic calendar | Calendared activity | Calendared activity |
| **Topics Covered** | Quiz 1 (L 1-4& T 1-1) **(CO1)** | Test 1  (L 1-14& T 1-5)  **(CO1-2)** | Comprehensive examination covering full syllabus. Students are expected to answer all questions **(CO1-5)** |
| Quiz 2 (L **5-9**& T 2-3) **(CO2)** |
| Quiz 3 (L 10-14& T 4-5) **(CO2)** | Test 2  (L 15-27& T 6-9)  **(CO3)** |
| Quiz 4 (L 15-22& T 6-7) **(CO3)** |

**Lesson Plan**

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| **L. No.** | **Topics** | **Course Outcome Addressed** |
| **L0** | Introduction to the course |  |
| **L1** | Brief overview of Logic gates, Truth Tables: AND OR, NOT, NAND, NOR, XOR gates, Sum-of-Products. | CO1 |
| **L2** | Sum-of-Products simplification, Product-of-Sums and its simplfication | CO1 |
| **L3** | Introduction to Verilog HDL, K map | CO1 |
| **L4** | K map simplification, Incompletely Specified Functions, Fan in, Factoring Functional decomposition, Multilevel NAND and NOR Circuits. | CO1 |
| **T1** | Functional decomposition, Multilevel NAND and NOR Circuits. Tutorial on k map | CO1 |
| **L5** | Addition of unsigned numbers- Half Adder, Full Adder | CO2 |
| **L6** | Ripple Carry Adder, Signed Numbers – Adder/Subtractor | CO2 |
| **T2** | Tutorial on signed and unsigned addition, Arithmetic Overflow, BCD Adder | CO2 |
| **L7** | Design of Arithmetic Circuits Using Verilog | CO2 |
| **T3** | Tutorial on Design of Arithmetic Circuits Using Verilog, Fast adder - Carry-Lookahead Adder | CO2 |
| **L8** | Carry-Lookahead Adder | CO2 |
| **L9** | Array multiplier | CO2 |
| **L10** | Arithmetic comparison circuits | CO2 |
| **L11** | Code converter | CO2 |
| **T4** | Tutorial on Code converter | CO2 |
| **L12** | Multiplexer | CO2 |
| **L13** | Decoder, Encoder | CO2 |
| **L14** | Verilog for Combinational Circuits | CO2 |
| **T5** | Tutorial on applications of multiplexers and decoders | CO2 |
| **L15** | Flip-Flops-RS | CO3 |
| **L16** | D, JK and T FF | CO3 |
| **L17** | Registers, Verilog for storage elements | CO3 |
| **L18** | Master/Slave FF | CO3 |
| **L19** | Edge triggered FF | CO3 |
| **T6** | Tutorial on FFs, Synchronous sequential circuits | CO3 |
| **L20** | Design of Synchronous Sequential Circuits- state assignment, state reduction | CO3 |
| **L21** | Moore-Mealy machines, | CO3 |
| **L22** | Design of synchronous counters | CO3 |
| **T7** | Tutorial on Design of Synchronous sequential circuits | CO3 |
| **L23** | Ripple Counters | CO3 |
| **L24** | Shift Registers | CO3 |
| **L25** | Ring and Johnson Counters | CO3 |
| **T8** | Tutorial on Verilog for counters | CO3 |
| **L26** | Algorithmic State Machine (ASM) Charts | CO3 |
| **L27** | Algorithmic State Machine (ASM) Charts-Examples | CO3 |
| **T9** | Tutorial on Algorithmic State Machine (ASM) Charts | CO3 |
| **L28** | Transistor Switches, NMOS, CMOS Logic Gates | CO1 |
| **L29** | Programmable Logic Devices, Noise Margin, Power dissipation, Transmission Gates, Fan-in, Fan-out in logic gates, Tri-state drivers | CO1 |
| **L30** | Bus Structure, Using Tri-State Drivers to Implement a Bus | CO4 |
| **T10** | Tutorial on Using Tri-State Drivers to Implement a Bus | CO4 |
| **L31** | Using Multiplexers to Implement a Bus | CO4 |
| **L32** | Verilog Code for Specification of Bus Structures-using tri state drivers | CO4 |
| **T11** | Tutorial on Verilog Code for Specification of Bus Structures-using multiplexers | CO4 |
| **L33** | Simple Processor | CO4 |
| **L34** | Simple Processor-Design | CO4 |
| **L35** | Simple Processor –Verilog code | CO4 |
| **L36** | A Bit-Counting Circuit- design | CO4 |
| **T12** | Tutorial on Bit-Counting Circuit-verilog code | CO4 |
| **L/T** | Click or tap here to enter text. |  |
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**References:**

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| 1. | Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design (3e), Tata McGraw Hill 2014. |
| 2. | Morris Mano M., Digital Design (2e), PHI Learning 2000. |
| 3. | Donald D. Givone, Digital Principles and Design, Tata McGraw Hill 2003. |
| 4. | F. Wakerly, Digital design - Principles and practice (4e), Pearson Education, 2013. |
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| **Submitted by:** | **Hemalatha S** |

**(Signature of the faculty)**

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| **Date:** | **29-07-2019** |

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| **Approved by:** | **Dr. Ashalatha nayak** |

**(Signature of HOD)**

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| **Date:** | **29-07-2019** |

**Faculty members teaching the course (IF MULTIPLE sections EXIST):**

|  |  |  |  |
| --- | --- | --- | --- |
| **FACULTY** | **Section** | **FACULTY** | **Section** |
| Dr. R. Vijaya Arjunan | A |  |  |
| Ms. Radhika Kamath | B |  |  |
| Ms. Musica Supriya | C |  |  |
| Dr. Hemalatha S | D |  |  |
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